Claim Amendments

1. (currently amended) A method for checking ~~electronic functionality of~~ a data bus between a first electronic module and a second electronic module operatively connected to the first electronic module, said method comprising:

conveying from the first electronic module to the second electronic module a first bit pattern through the data bus;

~~providing a second bit pattern in the second electronic module based on the first bit pattern as received in the second electronic module, the second bit pattern having a predetermined relationship with the received first bit pattern; and~~

receiving in the first electronic module ~~the~~ a second bit pattern from the second electronic module through the data bus; the second bit pattern contains at least a part of a reversed pattern of the first bit pattern;

comparing the received second bit pattern to the first bit pattern for determining a usable bus with of the data bus based a relationship between the first bit pattern and the reversed pattern of the first bit pattern.

2. (canceled)

3. (original) The method of claim 1, wherein the first bit pattern has an alternate pattern of '0' and '1'.

4. (original) The method of claim 1, wherein each bit in the received first bit pattern and the second bit pattern has a value of either '0' or '1', and second bit pattern is complement to the received first bit pattern such that a bit in the second bit pattern has a value different from the value of the corresponding bit in the received first bit pattern.

5. (currently amended) The method of claim 1 [[2]], wherein the first electronic module has a maximum bus width defined by a predetermined number of bits and the received second bit pattern has a section in which the pattern is complement to the corresponding part of the first bit pattern, said section having a further number of bits smaller than the predetermined number of

bits, and wherein said comparing step determines the usable width of the data bus based on the section in the received second bit pattern.

6. (currently amended) The method of claim 1, further comprising:

conveying to the second electronic module a third bit pattern through the data bus, wherein the third bit pattern contains at least a part of a reverse pattern of ~~is complement to~~ the first bit pattern; and

receiving from the second electronic module a fourth bit pattern through the data bus, the fourth bit pattern having the predetermined relationship to the third bit pattern as received in the second electronic module.

7. (original) The method of claim 6, further comprising

comparing the fourth bit pattern as received in the first electronic module to the third bit pattern for determining the usable bus width.

8. (original) The method of claim 1, wherein the second electronic module comprises a memory card.

9. (original) The method of claim 8, wherein the first electronic module has a maximum bus width and the memory card has a number of data pins, the number of data pins is equal to the number of bits conveyable on the maximum bus width.

10. (original) The method of claim 8, wherein the first electronic module has a maximum bus width and the memory card has a number of data pins, the number of data pins is smaller than the number of bits conveyable on the maximum bus width.

11. (original) The method of claim 8, wherein the first electronic module has a maximum bus width and the memory card has a number of data pins, the number of data pins is greater than the number of bits conveyable on the maximum bus width.

12. (currently amended) A software application product embedded in a computer readable medium ~~program~~ for use in a first electronic module for checking ~~electronic functionality of~~ a data bus between the first electronic module and a second electronic module, said computer readable medium having a plurality of executable codes ~~program~~ comprising:

a code for comparing

a first bit pattern provided to the second electronic module through the data bus to

a second bit pattern received through the data bus from the second electronic module, wherein the second bit pattern is provided in response to the first bit pattern as received in the second electronic module, the second bit pattern having at least a part of a reverse pattern of ~~a predetermined relationship to~~ the received first bit pattern.

13. (currently amended) The software application product ~~program~~ of claim 12, the executable codes further comprising

a further code, based on the predetermined relationship, for determining a usable bus width of the data bus for conveying data between the first electronic module and the second electronic module.

14. (currently amended) The software application product ~~program~~ of claim 12, wherein the received first bit pattern has an alternate pattern of '0' and '1' and the second bit pattern is complement to the received first bit pattern.

15. (currently amended) The software application product ~~program~~ of claim 12, further comprising a third code for generating the first bit pattern.

16. (currently amended) The software application product ~~program~~ of claim 13, wherein the first electronic module has a maximum bus width defined by a predetermined number of bits, and the received second bit pattern has a section in which the pattern is complement to the corresponding part of the first bit pattern, said section having a further number of bits smaller than the predetermined number of bits, and wherein the further code determines the usable width of the data bus based on the section in the received second bit pattern.

17. (currently amended) The software application product ~~program~~ of claim 13, wherein the code also compares

a third bit pattern provided to the second electronic module through the data bus to

a fourth bit pattern received through the data bus from the second electronic module, wherein the third bit pattern is complementary to the first bit pattern and the fourth bit pattern is provided in response to the third bit pattern as received in the second electronic module, and the fourth bit pattern having the predetermined relationship to the received third bit pattern, so as to allow the further code to determine the usable bus width of the data bus.

18. (currently amended) A memory unit for use in an electronic device, the electronic device having a host electronic module for processing data and a data bus for operatively connecting the host module to the memory unit, said memory unit comprising:

means for receiving a first bit pattern from the host module through the data bus; and

means, responsive to the received first bit pattern, for providing a second bit pattern on the data bus, wherein the second bit pattern has at least a part of a reverse pattern of ~~a predetermined relationship with~~ the received first bit pattern.

19. (currently amended) The memory unit of claim 18, wherein the host electronic module is adapted to compare the first bit pattern to the second bit pattern as received in the host module for determining a usable bus width of the data bus based on a complementary the predetermined relationship between the first bit pattern and the reversed pattern of the first bit pattern.

20. (original) The memory unit of claim 18, wherein the received first bit pattern has an alternate pattern of '0' and '1' and the second bit pattern is complement to the received first bit pattern.

21. (original) The memory unit of claim 19, wherein the data bus has a maximum bus width and the memory unit has a number of data pins for operatively connecting to the data bus, and

wherein the number of data pins is smaller than number of data bits conveyable in the maximum bus width.

22. (original) The memory unit of claim 19, wherein the data bus has a maximum bus width and the memory unit has a number of data pins for operatively connecting to the data bus, and wherein the number of data pins is equal to number of data bits conveyable in the maximum bus width.

23. (original) The memory unit of claim 19, wherein the data bus has a maximum bus width and the memory unit has a number of data pins for operatively connecting to the data bus, and wherein the number of data pins is greater than number of data bits conveyable in the maximum bus width.

24. (currently amended) An electronic device having means to receive a memory unit, comprising:

a data processing unit;

a data bus linking the data processing unit to the memory unit; and

a program for checking electronic functionality of the data bus, the program comprising:

a code for providing a first bit pattern to the memory unit through the data bus, and

a code for requesting the memory unit to provide a second bit pattern, the second bit pattern containing at least a part of a reverse pattern of the first bit pattern.

25. (currently amended) The electronic device of claim 24, wherein the program further comprises

a further code for comparing the first bit pattern with a second bit pattern as received through the data bus from the memory unit~~, wherein the second bit pattern is provided in the memory unit in response to the first bit pattern as received in the memory unit, the second bit pattern having a predetermined relationship to the received first bit pattern~~.

26. (currently amended) The electronic device of claim 25, wherein the program further comprises:

a third code for determining a usable width of the data bus based on the received second bit pattern based on a complementary ~~the predetermined~~ relationship between the first bit pattern and the reversed pattern.

27. (original) The electronic device of claim 24, wherein said program for checking the electronic functionality of the data bus is carried out at a boot up procedure.

28. (original) The electronic device of claim 24, comprising a mobile phone.

29. (original) The electronic device of claim 24, wherein said memory unit is disposed in a further electronic device.

30. (original) The electronic device of claim 24, wherein the memory unit comprises:

means for receiving the first bit pattern from the data process unit through the data bus; and

means, responsive to the first bit pattern as received through the data bus, for providing the second bit pattern on the data bus.

31. (original) The electronic device of claim 24, wherein the first bit pattern has an alternate pattern of '0' and '1'.

32. (original) The electronic device of claim 24, wherein each bit of the received first bit pattern and the second bit patterns has a value of either '0' or '1', and the second bit pattern is complement to the received first bit pattern.

[[32]]33. (currently amended) The electronic device of claim 26, wherein the program further comprises

a further code for providing a third bit pattern to the memory unit through the data bus, wherein the third bit pattern is complement to the first bit pattern, so as to allow the further code to compare the third bit pattern with a fourth bit pattern received through the data bus from the memory unit, the fourth bit pattern is provided in response to the third bit pattern as received in

the memory unit and the fourth bit pattern has the predetermined relationship to the received third bit pattern, and wherein the third code determines the usable width of the data bus also based on the received fourth bit pattern.